ARGUMENTS/ REMARKS

Favorable reconsideration of this application, as presently amended and in view of the following discussion, is respectfully requested.

Claims 1-17 are pending.

Claims 1, 2, 10, and 11 are presently amended, and Claims 14-17 are added. Support for the amendment to the original claims is found in the originally filed claims and in the specification at page 15, lines 11-12, for example. Support for new Claims 14-17 is found in the specification at page 17, lines 4-9, for example.

Before turning to the outstanding Office Action, Applicant first wishes to thank the Examiner for the courtesies extended during the personal interview of April 27, 2005. During the interview, the outstanding issues in the present application were discussed and arguments substantially as presented below were made. However, no agreement was reached with respect to the ultimate patentability of this application, pending the Examiner's further reconsideration and search.

In the outstanding Office Action, Claims 1-13 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,772,419 ("Sekiguchi") in view of U.S. Patent No. 5,623,677 ("Townsley"). Applicant respectfully traverses this rejection on the grounds that the amended independent claims, when considered as a whole, define inventions which are neither anticipated by nor obvious over the prior art.

As amended, independent Claim 1 defines an inventive processor power-saving control method. The method includes the step of interrupting a secondary operating system (OS) by issuing a secondary OS interrupt from the primary OS to the secondary OS when a task is to be executed on the secondary OS. The secondary OS is treated as a task to be performed by the primary OS. An advantage of the method of Claim 1 is that the secondary

OS does not necessarily require a separate hardware timer to generate interrupts . This makes it easier to efficiently maintain the power saving mode of the processor. (Specification at 3.)

Turning to the Sekiguchi reference, there is disclosed a multiple OS system. The system includes a main memory 102 with separate areas for an interrupt table 107, a first OS area 121, and a second OS area 122. (Sekiguchi at Figure 1.) The first OS area includes a page table 108, and the second OS area includes a page table 108'. (*Id.*) The interrupt table 107 maps a virtual address 401 of an interrupt handler to each interrupt number that the processor 101 receives from the interrupt controller 112. (*Id.* at column 6, lines 33-36.) The main memory also includes a common area 123 that includes the interrupt handler in the interrupt table 107. (*Id.* at Figs. 1, 2; column 16, lines 12-18.) When an external interrupt occurs, the interrupt handler determines whether the interrupt was issued by a device managed by the first OS or by the second OS. (*Id.* at column 16, lines 18-22.) If a device managed by the second OS issues the interrupt, the interrupt is processed by the second OS. (*Id.* at column 16, line 61 - column 17, line 22.) Accordingly, it can be appreciated that Sekiguchi does not disclose a secondary OS treated as a task to be executed by the primary OS where the secondary OS is interrupted by issuing a secondary OS interrupt from the primary OS to the secondary OS, as defined by Claim 1. Thus, Sekiguchi is not believed to anticipate or make obvious the invention of Claim 1.

Turning now to the Townsley reference, Townsley merely discloses a processor with a power saving mode. Nothing in Townsley teaches or suggests issuing a secondary OS interrupt from the primary OS to the secondary OS, as defined by Claim 1. Thus, Townsley, when considered alone or in combination with Sekiguchi, is not believed to anticipate or make obvious the invention of Claim 1.

Accordingly, Applicant submits that Claim 1 and all claims dependent therefrom patentably distinguish over the applied references. Since independent Claims 2, 10, and 11

define limitations similar to those found in Claim 1, Applicant also submits that Claims 2, 10, 11 and all claims dependent therefrom patentably distinguish over the applied references.

Attention is now directed to new Claims 14-17. Each of these claims defines the process of activating the secondary OS from a sleep mode in response to the secondary OS receiving the secondary OS interrupt from the primary OS, or a similar limitation. As explained during the interview, neither the Sekiguchi reference nor the Townsley reference discloses a secondary OS that is activated from a sleep mode in response to receiving a secondary OS interrupt from the primary OS. Accordingly, Applicant submits that Claims 14-17 patentably distinguish over the applied references for at least this additional reason.

In view of the foregoing discussion, no further issues are believed to be outstanding in the present application. Therefore, Applicant respectfully requests that this application be allowed and be passed to issue.

Respectfully submitted,

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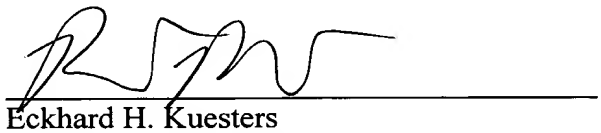

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